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EXAMINER
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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/188,241	Applicant(s) LUO, WENZHE	
	Examiner Terry L Englund	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,18,19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,18,19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *08 March 2001* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

The amendment submitted on Mar 8, 2002 was reviewed and considered with the following results:

The objection to Fig. 2, as described on page 1 of the previous Office Action, will be maintained until the examiner sees the proposed changes to the figure, or the change(s) are clearly described. The objection is described later under the appropriate section.

The objections to the disclosure, as described on page 3 of the previous Office Action, are also maintained. Even after reading lines 17-22 on page 7, the labeling of "switch MC" and "switch MS" are still not considered correct, and thus they are misleading and/or confusing. Details of the objections are described later under the Specification section.

The amended claims only overcame the rejections of claims 2 and 14 under 35 U.S.C. 112 with respect to their use of "current source." Those rejections have been withdrawn. Except for those two rejections, claims 1-14, 18, 19, 21,and 22 remain rejected under 35 U.S.C. 112 . These rejections are repeated later, with slight modifications related to the amendment's comments/arguments. The examiner's comments are described in the Response to Arguments section.

The prior art rejections of the claims have been modified to better clarify the "charge injection" limitation recited within the claims, and emphasized by the applicant's arguments/comments. These rejections, described later under their appropriate

section, include: 1) claims 1-5, 8-10, 12, 18, 19, 21, and 22 under 35 U.S.C. 103(a) with respect to Ravon; 2) claims 6, 7, and 11 under 35 U.S.C. 103(a) with respect to Ravon and the applicant's Prior Art Fig. 3; 3) claims 13 and 14 under 35 U.S.C. 103(a) with respect to Ravon; 4) claims 1-5, 8-10, 12, 18, and 19 under 35 U.S.C. 103(a) with respect to Harston; 5) claims 6, 7, and 11 under 35 U.S.C. 103(a) with respect to Harston and the applicant's Prior Art Fig. 3; and 6) claims 13 and 14 under 35 U.S.C. 103(a) with respect to Harston. Comments related to the prior art rejections, and the applicant's comments/arguments, are described under the Response to Arguments section.

Drawings

The drawings are objected to because it is not clear how Fig. 2 will actually be changed to "match the description in the Specification" as described on page 3 of the present amendment. It is assumed the change to Fig. 2 would show only VDD at the source of MS, and "Vo" would be shown at the drain of switch MS (i.e. common connection of MS and MC). However, without seeing the actual change, or having it clearly described, Fig. 2 is still objected to with respect to the "Vdd-Vo in Fig. 2" description on page 4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure remains objected to because of the following informalities: It is suggested "switch MC" on both lines 18 and 19 of page 7 be changed to --switch MS--.

Only then will the description clarify the current levels associated with the current source MC and switch MS shown in the applicant's Fig. 5. It is believed "a current level at the load side of the switch MC" is the same as the "current source side of the switch MC" because it is not clear what a "current source side" of a current source is. For example, it can be considered the side that sources current to subsequent circuitry. Therefore, both side descriptions appear to indicate the side of "switch MC" that corresponds to "A" shown in Fig. 5. This being the case, both sides will always have the same (equal) current. Also, the use of "switch MS", "switch MC", and "current source MC" is inconsistent and confusing. Therefore, appropriate corrections and/or clarifications are required which will help the examiner determine what the applicant is attempting to describe.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14, 18, 19, 21 and 22 remain rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is still not clear in independent claims 1 (line 6), 18 (lines 4-5), 21 (lines 8-9), and 22 (lines 9-10) what "to equalize a current level produced by said current source" means. For example, if the currents on both sides of a current source are (substantially) equal, it would be obvious to one of ordinary skill in the art that a MOS transistor used as a current source will have equal currents at its source and drain. Also, if the current source is providing a

predetermined, constant current, that current could be considered equal to its desired operational current. Since the applicant's own figures do not show how current would flow in the pull-down path, it is not clear how the current of the applicant's own current source is equalized.

The description "substantially continuously receives said current flowing from said current source" in claims 21 (lines 10-11) and 22 (lines 11-12) is still considered misleading. For example, the applicant's Fig. 5 shows current IA from current source 420 will flow to load 440 only when transistor switch 430 is conducting. However, when transistor switch 430 is open, current IA cannot flow from the current source to the load. Therefore, how can the load "substantially continuously" reduce charge injection when switch 430 is open? Since current IA would then be flowing through (or into) the pull-down mirror path, no current or charge injection would be "flowing to" the load. However, as long as switch 430 is closed, the load will always receive the current flow from the current source unless the load is allowed to become fully charged, and at that time, current flow would then cease. Also, as long as switch 430 is closed, there will be no charge injection related to switch 430 because of the lack of switching operations.

Dependent claims carry over the rejection from their respective independent claim.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 1-5, 8-10, 12, 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon, a reference cited in the previous Office Action. For the following descriptions, Figs. 2-4 of Ravon will be considered and/or referred to, wherein one of ordinary skill in the art would be able to recognize the relationships between the figures. In Fig. 2, Ravon shows a current source switching circuit comprising a current source 11; transistor switch M1; what can be deemed a pull-down mirror path M2,13,14 in parallel with transistor switch M1 (e.g. they are both coupled between terminal E and ground); and first load C',2. Current source 11 is shown in detail in Fig. 3 (see column 4, lines 44-45), and is disclosed as providing a constant current I (e.g. see column 3, line 31 and column 4, lines 44-45). Fig. 4 shows part C' of first load C',2, transistor M2, and details of comparator 14. Although transistor switch M1 is replaced by diode D1 in Fig. 4 (see column 6, lines 16-18), Ravon also discloses a transistor provides better efficiency on column 6, lines 24-25. Therefore, for the following description, diode D1 of Fig. 4 will be replaced with a transistor switch (e.g. M1 of Fig. 2) for improved efficiency, wherein block 13 of Fig. 2 will be used to control the on/off operations of both transistors M1 and M2. One of ordinary skill in the art would recognize that current source 11 (shown in Figs. 2 and 3) provides current I to terminal E of Fig. 4. Although the reference does not clearly

disclose the "substantially continuously" reduction of "charge injection" as recited within the claims, one of ordinary skill in the art would know it relates to the current received by the load C',2 from the current source when transistors M2 and M1 are switched off and on. For example, when transistor M2 is switched off and transistor switch M1 is switched on, first load C',2 receives current I (from current source 11) through transistor switch M1 (e.g. see Fig. 2). Besides charging first load part C', the current also charges capacitor C1 through resistor R1 (see Fig. 4). [Note that the structure of first load C',2, capacitor C1, resistor R1, and amplifier 20 closely corresponds to the respective load 440, capacitor C1, resistor R1, and amplifier 400 structure of the applicant's Fig. 5.] When transistor switch M1 is switched off, and transistor M2 is switched on, capacitor C1 will help maintain the voltage across first load C',2 (i.e. between terminal S and ground). Therefore, less current will be required to completely charge first load C',2 back up once transistor switch M1 is switched back on. Also, since current I is constant, the current flowing through M2 will be equal to the current flowing through M1, when the respective transistor is conducting (i.e. switched on). After switching switch M1 on and M2 off, transistor switch M1 and pull-down mirror path M2,13,14 will substantially continuously reduce the charge injection into first load C',2. For example, when switch M1 is switched off and switch M2 is switched on, current I does not flow to load C',2, but flows through switch M2. Therefore, there will be no current I flow into load C'.2 from current source 11, and charge injection "flowing to" the load is reduced. When switch M1 is switched on and switch M2 is switched off, current I will flow to load C',2, until the load is fully charged, or until M1 and M2 are switched into their off and on states,

respectively. Therefore, during the periods when switches M1 is held in the on and the off states, charge injection is substantially continuously reduced, rendering claim 1 obvious. [The voltage at terminal S will be basically maintained across first load C',2 by the voltage held across capacitor C1, when switch M1 is not conducting. Therefore, once switch M1 is switched on, current I will flow through switch M1 and into load C',2 without any abrupt changes of voltage and current, thus reducing charge injection related to the switching operation.] Fig. 2 clearly shows current source 11 connected between power source Vc and a first side (i.e. terminal E) of transistor switch M1, and first load C',2 connected between ground and a second side (i.e. terminal S) of transistor switch M1, thus claims 2 and 3 are rendered obvious. Since first load C',2 has a charging capacitor C', and transistor M1 is a MOS transistor, claims 4 and 5 are rendered obvious. Transistor M2 of the pull-down mirror path M2,13,14 can be deemed a pull-down amplifier (e.g. transistors can be deemed one type of an amplifier), rendering claim 8 obvious. When transistor M2 is conducting, its output (i.e. drain) follows the current source 11 side of the transistor switch M1 by allowing the current to flow through transistor M2, thus claim 9 is also rendered obvious. Transistors M1 and M2 receive their respective signals from control 13 (see Fig. 2) which allows transistor M2 to be turned off, and then transistor M1 to be turned on (see column 4, lines 28-30). Therefore, transistor M2 is deemed a complementary pull-down mirror path transistor switch, which operates opposite the transistor switch M1 at that point of operation, rendering obvious claim 10. Since current source 11 comprises MOS transistor M3 (e.g. see Fig. 3), claim 12 is rendered obvious. Transistor/switch M2 provides a pull-down

mirror path parallel with current switch M1 (e.g. coupled between terminal E and ground), wherein switches M2 and M1 are substantially turned on and off alternatively, rendering obvious claims 18 and 19 because when transistor M1 is off, the capacitor C1 will basically maintain a voltage on load capacitor C', thus substantially continuously reducing the charge injection flowing to the load (e.g. no current) while equalizing the current flow (e.g. current I will flow through either M1 or M2, depending on which one is conducting) as previously explained above. Transistor switch M1 connects current source 11 to load C',2, and it is substantially simultaneously turned off when switch M2 is turned on. When switch M2 is on, the current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C',2, the charge injection will be reduced when transistor switch M1 is switched off, rendering obvious claim 21. The upper output of block 13 is coupled to the gate of transistor switch M1 and is deemed the means for switching open transistor switch M1, and the lower output of block 13 is coupled to the gate of switch M2 and is deemed the means for switching close switch M2, wherein current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C',2, the charge injection will be substantially continuously reduced when transistor switch M1 is switched opened, rendering claim 22 obvious.

Claims 6, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to respective claims 1 and 10 above, and further in view of the applicant's Prior Art Fig. 3. As described previously, the basic current source switching

circuit is shown and disclosed by the reference of Ravon. However, the reference does not show or disclose the use of the serial combinations of transistors as recited within claims 6, 7 and 11. Ravon shows only a single transistor for transistor switch M1 and one transistor for complementary pull-down mirror path transistor switch M2. It would have been obvious to one of ordinary skill in the art to replace each of transistors M1 and M2 of Ravon's circuit with a respective compensated transistor switch of the applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection. Since Ravon's circuit can be considered a current type switch circuit for charging first load C',2, the compensated switch of the applicant's Fig. 3 would help reduce charge injection even more within the circuit if that was desired.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to claim 1 above. As described previously, Figs. 2 and 4 of Ravon show a circuit with a transistor switch M1, pull-down mirror path M2,13,14, current source 11, and first load C',2. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuitry of Ravon by reversing the polarities

(i.e. Vc and ground would be reversed) and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage (e.g. closer to power source Vc). The reversal would replace all the MOS transistors (i.e. M1-M6) with their complementary transistors (i.e. an NMOS transistor would be replaced with a PMOS transistor). In this case, transistor M2 would be coupled between power source Vc and the common connection of current source 11/transistor switch M1, and first load C',2 would be coupled between power source Vc and terminal S. Therefore, transistor M2 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 11 would be coupled between ground and one side (i.e. terminal E) of transistor switch M1, rendering obvious claim 14.

In so far as being understood, claims 1-5, 8-10, 12, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harston, another reference cited in the previous Office Action. In Fig. 3 Harston shows a current source switching circuit comprising current source MP1; transistor switch MP2; a pull-down mirror path MP3 in parallel with transistor switch MP2; and first load 10pf. Although the reference does not clearly disclose a substantially continuously reduction in charge injection, it would be obvious to one of ordinary skill in the art that resistor 37.5Ω, and the switching operations of MP2 and MP3, would substantially continuously reduce the charge injection flowing to first load 10pf. For example, when transistor switch MP2 is off, the current from current source MP1 will flow through MP3 to ground. Since the current that flows through MP2 and MP3 is from the same current source, they are deemed equalized. Also, when current is flowing through MP3 (and not MP2), and there is still a

charge on first load 10pf, the current flowing to the first load will be reduced because the load will be disconnected from the current source, and current will actually flow from the load through the resistor. After transistor switch MP2 is initially switched back on, there will be a substantially continuously reduction of charge injection flowing to load 10pf because when there is no switching, there is no charge injection occurring (with respect to the switching operation), and current will flow from current source MP1 to load 10pf. Therefore, claim 1 is rendered obvious. [MP3 is considered a pull-down mirror path since it mirrors the operation of the transistor switch MP2 and allows the current from transistor MP1 to flow down to ground when switch MP2 is not conducting. See column 2, lines 64-68.] Fig. 3 also shows a current source MP1 (a MOS transistor) coupled between power source CURRENT CELL and the first side of transistor switch MP2; and load 10pf is a charging capacitor 10pf coupled between ground and a second side of transistor switch MP2, thus rendering obvious claims 2-5. Since a transistor can be deemed an amplifier, pull-down mirror path MP3 can be deemed a pull-down amplifier, rendering claim 8 obvious. When transistor MP3 is conducting, its output (i.e. drain) follows the current source MP1 side of the transistor switch MP2 by allowing the current to flow through transistor MP3, thus rendering obvious claim 9. Transistors MP2 and MP3 receive their respective signals DATAB and DATA. Therefore, transistor MP3 can be deemed a complementary pull-down mirror path transistor switch operating the opposite of transistor switch MP2, rendering claim 10 obvious. It is complementary since it receives a control signal which is a complement of the signal received by transistor switch MP2. Since current source MP1 is a MOS transistor, claim 12 is

rendered obvious. Transistor/switch MP3 provides a pull-down mirror path parallel with current switch MP2, wherein switches MP3 and MP2 are alternatively on and off, rendering obvious claims 18 and 19 because when transistor MP2 is off, the resistor 37.5Ω will discharge load 10pf, thus substantially continuously reducing the charge injection flowing to the load as previously described. For example, when the load capacitor is discharging, the current will flow away from the load. Therefore, there will be no charge injection flowing to the load, and the charge injection will be substantially continuously reduced as long as MP2 is not conducting. Also, when MP2 begins conducting before load capacitor 10pf has completely discharged through resistor 37.5Ω, the current (e.g. charge injection) required to charge the load capacitor back up will be less, and as long as switch MP2 is on, the charge injection will be reduced. Therefore, it would be obvious to one of ordinary skill in the art that the charge injection flowing to the load, under the conditions described above, can still be considered substantially continuously reduced.

Claims 6, 7, and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to their respective claim 1 or 10 described above, and further in view of the compensated transistor switch of the applicant's Prior Art Fig. 3. Harston shows only a single transistor for each of transistor switch MP2 and complementary pull-down mirror path transistor switch MP3. It would have been obvious to one of ordinary skill in the art to replace each of the single transistors MP2 and MP3 of Harston's circuit with a respective compensated transistor switch of the applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial

combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection of switches in analog circuits. Since Harston's circuit in Fig. 3 can be considered a current switch circuit related to an analog circuit, the compensated switch of Fig. 3 would help reduce charge injection within the circuit if that was desired.

Claims 13 and 14 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to claim 1 above. As described previously, Fig. 3 of Harston shows a circuit with a transistor switch MP2 (30), pull-down mirror path MP3 (32), current source MP1 (20), and load capacitor 10pf. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuit of Fig. 3 by reversing the polarities and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage. The reversal would replace all the PMOS transistors (i.e. MP1, MP2 and MP3) with NMOS transistors. In this case transistor 32 would be coupled between power source CURRENT CELL and the common connection of current source 20 and transistor switch 30. Therefore, transistor 32 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 20

would be coupled between ground and one side of transistor switch 30, rendering obvious claim 14.

No claim is allowable. Claims 15-17, and 20 had been canceled previously.

Response to Arguments

The applicant's arguments filed Mar 8, 2002 have been fully considered but they are not persuasive. The applicant argues: 1) the labeling of the switches on page 7 are correct; 2) the current source is equalized with respect to itself; 3) the claim as a whole must be considered with respect to the load that "substantially continuously" receives current; 4) the applicant claims the invention broadly, and the claim language is to be considered as a whole, not out of context; 5) Ravon's system has varying currents and limits transient variations; 6)(a) the applicant's current source is capacitive, wherein Ravon's current source is not, (b) the current paths have matched impedance, and (c) the current source is switched on and off; 7)(a) the references don't mention charge injection, and therefore fail to teach reduction of charge injection, (b) the current flow to ground of Harston performs no useful purpose, and is not for reducing charge injection, and (c) Harston simply changes state of a DAC, and with a constant current, wouldn't produce charge injection from switching; 8) any current source associated with charge injection would be covered by the claimed invention; 9) AAPA fails to teach charge injection by a pull-down mirror path, and teaches an unsatisfactory circuit for charge injection; and 10) the pull-down mirror path reduces charge injection.

1) Although the applicant's comments on page 3 of the amendment indicate the labeling of the switches on page 7 are correct, the examiner disagrees. For example,

why is "MC" identified as a "switch" on lines 18 and 19, and then as a "current source" on line 21? Also, since current flowing through switch (transistor) MC will have minimal loss due to leakage current within the transistor, the current level at the source of MC is considered equal to the current level at its drain, the load side of current source MC. Therefore, how does the applicant actually equalize the current on both ends of current source MC? Plus, what is considered the "current source side of switch MC" since MC is the current source itself? Also, if "switch MC is a switched current source" as page 3 of the amendment indicates, what causes it to switch? Only when it is combined with switches MS and/or MT would it be considered a "switched current source" by the examiner. Without at least one of those switches, MC is shown as a constant current source due to the reference voltage applied to its gate. Therefore, consistent labeling within the disclosure would minimize confusion, and also help identify what the applicant is actually trying to convey.

2) Related to #1 above, the applicant states the current source is equalized with respect to itself, and the references fail to mention or teach the current level of the current source is equalized. However, is the applicant considering their own current source MC (e.g. see the applicant's Fig. 5) would be the current source, or is it the combination of MC and MS that is to be considered the current source? If only MC is considered the current source, it is obvious to one of ordinary skill in the art that the current flowing through its source will also be equal (or substantially equal) to the current flowing through its drain. If the combination of MC and MS is considered the current source, the current flowing through either the drain or source of MC does not

appear to be actually equalized to the current flowing on the load side of MS when MS is open. It is believed the voltage potential on both sides of the transistor switch are basically maintained as substantially the same level. As with #1 above, consistent labeling would help minimize confusion with respect to what is considered the current source of the invention. Also, it is noted that MPEP 2111 describes "claims must be given their broadest reasonable interpretation." A MOS configured current source, whether identified as constant or not, is easily interpreted by one of ordinary skill in the art as one type of current source providing an equalized current (e.g. same current flowing through its source and drain; or a current, equal to its desired, operational level, to flow). Even the applicant admits "a current source at its desired operational current...could possibly be the ultimate result of equalization" on page 4 of the amendment. Therefore, that is one type of equalized current under the "broadest reasonable interpretation" as described in MPEP 2111.

3) The applicant indicates "the entire claim language" must be considered with respect to "continuously receives said current flowing from said current source." However, even the applicant's own load 440 can only receive current IA from current source 420 when switch 430 is closed (see Fig. 5). In the applicant's arguments/ comments, the applicant cites "a load that "substantially continuously" receives current" on page 5. This description does not correspond to the limitation (in claims 21 and 22) actually claimed, wherein the claims recite "said load substantially continuously receives said current flowing from the current source." Therefore, between the applicant's arguments/comments, and the actual claimed limitation, it is not clear if the applicant

intends that the load merely has to receive some type of current, or the current actually provides by the current source. Since the examiner determines patentability on the claimed invention, and not on any alleged limitation(s) being read into the claim, it is suggested the claims be carefully reviewed and modified to clearly cite limitations the applicant's own circuit and disclosure can support. For example, unless the applicant can support the "load substantially continuously receives said current flowing from the current", that limitation is not supported by the disclosure.

4) The applicant admits the current source is claimed broadly, and then indicates the examiner must consider the claimed invention as a whole, and not taken out of context. However, if the claim language is not clear, or possibly not even supported by the applicant's own figures and disclosure as presently claimed (and previously described), the examiner must use his/her experience to consider the claimed limitations of the invention under their "broadest reasonable interpretation" (MPEP 2111). In the applicant's own invention (e.g. see Fig. 5), current IA from current source 420/MC is either directed to load 440/CL when switch 430/MS is closed, or allowed to flow into another path 450 when switch 430/MS is opened. It is the switching operation between those two current paths that reduces charge injection to the load. However, in both Ravon and Harston, they also show current from a current source being either routed to the load or switched to another path. Since the applicant admits charge injection only exists for a very short time when current is allowed to flow to a load (see page 5 of the amendment), it is not understood why the prior art references will not have reduced charge injection since they switch current flow to, and away from, the load as

well. For example, once current is switched to flow to the load, what would prevent charge injection from being substantially continuously reduced in those references if no more switching action occurs? Therefore, it appears the applicant wants to claim limitations broadly, not have them taken out of context, but then believes prior art references must be narrowly interpreted. In this case, it appears the applicant wants to interpret the claimed invention's limitations to include limitations which are not clearly recited within the claims, wherein it is now believed the applicant is actually taking the claimed limitations out of context. Therefore, the examiner requests clarification on why the examiner's "broadest reasonable interpretation" (as described within MPEP 2111) is not acceptable to the applicant in view of the presently worded claims.

5) The applicant argues Ravon's system has varying currents and limits transient variations. Ravon clearly indicates current source 11 provides a constant current I (see column 3, line 31 and column 4, line 44-45) which is the current allowed to flow to load C',2 when switch M1 is closed, or to ground when switch M2 is closed and switch M1 is open. Since the system of Ravon helps to eliminate transients of the voltage supply to the load, those transients can affect the switching operation of switches M1 and M2. Therefore, it is believed by eliminating those transients, and helping to maintain a constant current, the charge injection (related to the switching operation within the circuit) is reduced to the load of Ravon's circuit.

6) In response to applicant's argument that the references fail to show certain features of the applicant's invention, it is noted that the features upon which the applicant relies (i.e., (a) the current source is capacitive; (b) the current paths have

matched impedances; and (c) the current source is switched on and off) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). (a) Since the current source of both Ravon and Harston contain at least one MOS transistor (e.g. Ravon's M3,M4 and Harston's MP1), and clearly show a capacitive load (e.g. Ravon's C' and Harston's 10pf), it is believed each reference's current source will have a capacitance (e.g. gate to source; gate to drain) and can be considered a type of capacitive current source. If this is not the case, the examiner requests clarification on how the applicant's own current source (e.g. Fig. 5: 420/MC) might be considered a capacitive current source, wherein neither of the prior art references do not show/ disclose one. (b) None of the claims recite anything about matched impedances within each current path. (c) With respect to the applicant's argument on page 12 that the references do not show a current source that is turned on and off, it must be pointed out that the applicant's own current source (e.g. see 420/MC of Fig. 5) is not turned on and off. For example, the applicant's own current source 420/MC (see Fig. 5) does not switch. Switches MT and MS are the means to switch/divert the current source's current IA to either load 440/CL or into path 450. It is those switching operations that can produce charge injection, not the actual switching on and off of the current source itself. The current source just continuously provides current IA to either one of the two current paths. Since both Ravon and Harston have a switch coupled between the current source and load, and another switch to divert the current flow away from the load, those switches can produce charge

injection (e.g. spikes) when they are initially turned on and off. If the applicant believes 420/MC and switches 430/MS and 450/MT comprise the current source (see Fig. 5), the current source is still not turned off and on. It is always providing current IA. If the applicant believes 420/MC and 430/MS comprises the current source, its current flow to the load can be turned on and off due to the switching action of 430/MS. However, what would then be considered the transistor switch between the current source and the load that supposedly turns off the current flow to the load?

7) (a) Since the references do not mention charge injection, they fail to teach its reduction according to the applicant's arguments/comments. Apparently, the applicant relies on a narrow interpretation of the prior art, basically insisting the references clearly show/disclose "charge injection" reduction. However, one of ordinary skill in the art is allowed the "broadest reasonable interpretation" of the prior art references. Due to the similarities of the references and the applicant's own circuit (i.e. one current source providing current to either one of two current paths during certain switching operations, wherein one path allows the current to flow to the load and the other allows it to flow somewhere other than to the load), it would be reasonable to one of ordinary skill in the art to interpret those references as showing/disclosing circuitry that does reduce charge injection without having to specifically state it. The reasoning behind why the charge injection limitation recited within the clams is met by the prior art reference cited is described in detail within the rejections and/or previous comments. (b) The current flow to ground in Harston's circuit performs no useful purpose and does not reduce charge injection. However, it is believed that as long as the current source's current is diverted

away from the load, the charge injection will be reduced during the switching operation. Also, as long as the current source is always providing a current flow to some current path, when the current is switched back to the load, there will be no abrupt change in the output of the current source itself. Its current will be merely rerouted from one current path to another, thus leaving the current source to continuously provide the flow of current. Otherwise, if the current source itself is either turned off, or given no path for its current to flow, there will be a temporary surge of current from its output once the current source is turned back on, or the current source's output is given a current path which allows the flow of current. This initial, and abrupt current surge can cause unnecessary charge injection into the load. Therefore, allowing the current source to continually provide a current will help reduce charge injection. (c) Harston's circuit changes the state of a DAC and doesn't produce charge injection from switching. Since the applicant admits Harston's circuit doesn't produce charge injection (see page 10 of the amendment), isn't that an admittance that the circuit has reduced charge injection in the sense that if there is no charge injection, it has been reduced to zero? However, in another line of thought, it is believed the actual switching between the current flowing into the load to flowing through another path, and vice versa, can create the charge injection. Therefore, wherever there is switched current, charge injection can occur, and it is believed Harston's circuit does help to reduce it by keeping current source MP1 continuously providing a current flow through one of the two paths as previously described. Since Harston's circuit switches current away from a DAC, the switching action that still allows the continuous current flow, is one way to minimize charge

injection. If considering charge injection only occurs during actual switching operations, as long as current is left flowing to the load, charge injection is reduced because of the lack of any type of switching operation during that time period.

8) The applicant admits "any current source that is associated with charge injection would be covered by Applicant's claimed invention" on page 8 of the amendment. Again, the examiner believes the applicant wants to claim broadly, but then other prior art must be narrowly interpreted with respect to the applicant's own invention. However, this type of reasoning does not correspond to the knowledge of one of ordinary skill in the art, and the examiner's support from MPEP 2111 with respect to the "broadest reasonable interpretation."

9) In response to the applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the applicant argues the applicant's admitted prior art (AAPA) fails to teach charge injection by a pull-down mirror path, and teaches an unsatisfactory circuit for charge injection. However, the applicant's own admitted prior art descriptions indicate the circuits can be used to reduce charge injection (e.g. see "used to cancel any potential charge injection" and "even the use of compensated switches do not solve the problem of charge injection completely" on page 3, lines 25-26 and 28-30, respectively of the disclosure). Therefore, the applicant's own prior art descriptions indicate compensated switches (e.g. shown in the applicant's Fig. 3) can be useful for

reducing charge injection. Since the examiner's rejections clearly combine AAPA Fig. 3 with a reference that clearly show/disclose a pull-down mirror path in parallel with a transistor switch for providing current to a load (when it is closed/conducting), and the rejections also provide motivation for the combination of the references, the AAPA reference cannot be attacked individually.

10) Related to some of the other arguments/comments above, the applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Although the applicant indicates the pull-down mirror path reduces charge injection in the claimed invention, both the references of Ravon and Harston show what can be deemed a pull-down mirror path coupled in parallel with the transistor switch. Since the current from the current source is diverted through either the pull-down mirror path or the transistor switch due to their respective switching operations, it is believed charge injection caused by the switching action can occur. This charge injection will be reduced as previously described. If the applicant disagrees, the examiner requests clarification with respect to the applicant's actual claim language and circuit operation, and well as why the references of Ravon and Harston do not read on the claim language, as presently written.

Due to the confusion related to the claim language, what the applicant indicates is claimed (versus what is actually claimed), and similarities with the prior art references

as described above, the rejections within the previous, and the present, Office Actions are deemed proper.

THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund
2 June 2002

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800